PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re	:	Application of Yones
For	:	**POWER-ON RESET FOR TRANSPONDER**
Serial No.	:	
Filed	:	Concurrently herewith
Group Art Unit	:	
Examiner	:	
Our Docket No.	:	DN1999116USA

November 15, 2001

ASSISTANT COMMISSIONER OF PATENTS
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

This is a preliminary amendment filed with a 35 U.S.C. 365 filing of a PCT International Application designating the United States.

Please amend the referenced application as follows:

IN THE CLAIMS

Please cancel claims 1-18 and replace with claims 19-36 as follows:

19. An RF transponder comprising a plurality of circuits, a power supply for providing power, including an input voltage, to the plurality of circuits, and a one of the plurality of circuits comprising a Power-On Reset circuit for generating a reset signal for maintaining other ones of the plurality of circuits in an inoperative reset mode unless the power supply has sufficient power to ensure proper operation of the other ones of the circuits, the RF transponder characterized in that:

at least one of the other ones of the plurality of circuits comprises control logic which, upon release of the reset signal, starts transmission of a data stream at a first bit of the data stream, in order to ensure a first-pass transmission of a complete data stream.

20. An RF transponder, according to claim 19, characterized by:

a flip-flop circuit for setting and clearing a state of the reset signal; and

an init delay circuit, connected to an input of a comparator, for controlling the flip-

flop circuit so that the flip-flop circuit holds the reset signal in an ON-state for a delay time after abrupt power-up of the transponder.

21. An RF transponder, according to claim 19, characterized by:

a flip-flop circuit for setting and clearing a state of the reset signal; and

a voltage divider connected to a first comparator, for providing an input signal to a voltage limit circuit; wherein the voltage limit circuit controls the flip-flop circuit so that the flip-flop circuit sets the reset signal in response to the input voltage being less than or equal to a minimum sustaining voltage, and clears the reset signal in response to the input voltage being greater than the minimum sustaining voltage.

22. An RF transponder, according to claim 21, characterized in that:

the minimum sustaining voltage has different values, in different transponder operating modes.

23. An RF transponder, according to claim 22, characterized in that:

in an active transponder operating mode, the power supply derives power for the plurality of circuits from a battery; and

in a passive transponder operating mode, the power supply derives power for the plurality of circuits from an RF signal received by an antenna system.

24. An RF transponder, according to claim 21, characterized by:

a second comparator connected to the voltage divider and providing an input signal to the voltage limit circuit; wherein the voltage limit circuit controls the flip-flop circuit so that the flip-flop circuit sets the reset signal while the input voltage is increasing from less than or equal to a minimum sustaining voltage to a minimum starting voltage, and clears the reset signal when the input voltage increases above the minimum starting voltage.

25. An RF transponder, according to claim 24, characterized by:

logic in the voltage limit circuit for combining the input signal from the first comparator and the input signal from the second comparator so that, after the input voltage has increased above the minimum starting voltage, the flip-flop circuit maintains a cleared reset signal state as long as the input voltage remains above the minimum sustaining voltage, and so that after the input voltage has increased above the minimum starting voltage, the flip-flop circuit sets the reset signal when the input voltage decreases to less than or equal to the minimum sustaining voltage.

26. An RF transponder, according to claim 21, characterized by:

an init delay circuit connected to an input of a second comparator which shares control of the flip-flop circuit with the voltage limit circuit, so that the flip-flop circuit holds the reset signal in an ON-state after the beginning of power-up for a longer one of a first period of time which is a delay time and a second period of time which is a time expended while the input voltage increases to greater than a minimum voltage.

27. An RF transponder, according to claim 19, characterized by:

an input for an external reset signal; and

at least one logic element, for combining the external reset signal with the Power-On Reset-generated reset signal and forming a combined reset signal, wherein the combined reset signal is set in response to either the external reset signal or the Power-On Reset-generated reset signal being set, and the combined reset signal is cleared when the external reset signal and the Power-On Reset-generated reset signal are both clear.

28. An RF transponder, according to claim 27, characterized by:

a gate connected between ground and the input for the external reset signal, wherein the gate is controlled by a one of the power supply voltages so that the external reset signal is cleared when the power supply voltage is at a level suitable for logic control.

29. An RF transponder, according to claim 19, wherein:

the power for the Power-On Reset circuit is the highest available regulated voltage (Vxx); and components of the Power-On Reset circuit are selected for minimal power use and for operation at the lowest possible voltages, so that the Power-On Reset circuit is functional before the other ones of the plurality of circuits, characterized in that the Power-On Reset circuit comprises:

low current, three-stage comparators;

Schmitt trigger inverters; and

a low current voltage divider, utilizing on-chip, high value poly resistances.

30. Method of controlling operation of an RF transponder during power-up and power-down, wherein the RF transponder comprises a plurality of circuits, a power supply for providing power, including an input voltage, to the plurality of circuits, and a Power-On Reset circuit for generating a reset signal for maintaining selected ones of the plurality of circuits in an inoperative reset mode unless the power supply has sufficient power to ensure proper operation of the plurality of circuits, the method characterized by:

upon release of the reset signal, starting data transmission with a first bit of a data stream to be transmitted, in order to ensure a first-pass transmission of a complete data stream.

31. Method, according to claim 30, characterized by:

holding the reset signal on for a delay time after abrupt power-up of the transponder.

32. Method, according to claim 30, characterized by:

selecting a value for a minimum sustaining voltage to different values for transponder operation based on different operating modes for the RF transponder.

33. Method, according to claim 32, characterized in that:

in an active transponder operating mode, the power supply derives power for the plurality of circuits from a battery; and

in a passive transponder operating mode, the power supply derives power for the plurality of circuits from an RF signal received by an antenna system.

34. Method, according to claim 30, characterized by:

holding the reset signal in an ON-state after the beginning of power-up for a longer one of a first period of time which is a delay time and a second period of time which is a time expended while the input voltage increases to greater than a minimum voltage.

35. Method, according to claim 30, characterized by:

setting a combined reset signal when either an externally-supplied reset signal or the transponder-generated reset signal is set; and

clearing the combined reset signal when both the external and the transponder-generated reset signals are clear.

36. Method, according to claim 35, characterized by:

clearing the externally-supplied reset signal whenever the voltage level of the power supply is suitable for digital logic control.

REMARKS

The claims have been amended to delete the numbers identifying elements, which were originally incorporated to comply with PCT practice. A separate copy of the claims as amended is included for the Examiner's convenience.

Favorable examination and consideration are respectfully requested.

Respectfully submitted,

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Claims:

19. An RF transponder comprising a plurality of circuits, a power supply for providing power, including an input voltage, to the plurality of circuits, and a one of the plurality of circuits comprising a Power-On Reset circuit for generating a reset signal for maintaining other ones of the plurality of circuits in an inoperative reset mode unless the power supply has sufficient power to ensure proper operation of the other ones of the circuits, the RF transponder characterized in that:

at least one of the other ones of the plurality of circuits comprises control logic which, upon release of the reset signal, starts transmission of a data stream at a first bit of the data stream, in order to ensure a first-pass transmission of a complete data stream.

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the power for the Power-On Reset circuit is the highest available regulated voltage (Vxx); and components of the Power-On Reset circuit are selected for minimal power use and for operation at the lowest possible voltages, so that the Power-On Reset circuit is functional before the other ones of the plurality of circuits, characterized in that the Power-On Reset circuit comprises:

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upon release of the reset signal, starting data transmission with a first bit of a data stream to be transmitted, in order to ensure a first-pass transmission of a complete data stream.

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32. Method, according to claim 30, characterized by:

selecting a value for a minimum sustaining voltage to different values for transponder operation based on different operating modes for the RF transponder.

33. Method, according to claim 32, characterized in that:

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clearing the combined reset signal when both the external and the transponder-generated reset signals are clear.

36. Method, according to claim 35, characterized by:

clearing the externally-supplied reset signal whenever the voltage level of the power supply is suitable for digital logic control.